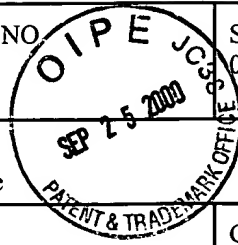


| Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | | | ATTY DOCKET NO. 0325.00372 | | | | SERIAL NO. 09/605,325 | | | |
|---|---|-----------|---------------------------------|--------------------------------|---------------|-------------------|--|---|--|--|--|
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | | | | APPLICANT: Michael T. Moore | | | | <div style="display: flex; flex-direction: column; align-items: center;"> <div style="border: 1px solid black; border-radius: 50%; padding: 5px; text-align: center; margin-bottom: 5px;"> O I P E SEP 25 2000 PATENT & TRADEMARK OFFICE </div> <div style="writing-mode: vertical-rl; transform: rotate(180deg); font-weight: bold;"> RECEIVED SEP 27 2000 TC 2700 MAIL ROOM </div> </div> | | | |
| | | | | FILING DATE June 28, 2000 | | | | | | | |
| U.S. PATENT DOCUMENTS | | | | | | | | | | | |
| Examiner Initial | Document No. | Date | Name | Class | Sub- Class | Filing Date | | | | | |
| MN | 4 0 5 1 3 5 2 | 9/27/1977 | Eichelberger et al. | 364 | 716 | | | | | | |
| MN | 4 9 4 0 9 0 9 | 7/10/1990 | Mulder et al. | 307 | 465 | | | | | | |
| MN | 5 2 0 4 6 6 3 | 4/20/1993 | Lee | 340 | 825.34 | | | | | | |
| MN | 5 2 3 7 6 9 9 | 8/17/1993 | Little et al. | 395 | 750 | | | | | | |
| MN | 5 2 4 1 2 2 4 | 8/31/1993 | Pedersen et al. | 307 | 465 | | | | | | |
| MN | 5 2 6 8 5 9 8 | 12/7/1993 | Pedersen et al. | 307 | 465 | | | | | | |
| MN | 5 2 8 7 0 1 7 | 2/15/1994 | Narasimhan et al. | 307 | 465 | | | | | | |
| MN | 5 3 8 4 4 9 9 | 1/24/1995 | Pedersen et al. | 326 | 39 | | | | | | |
| MN | 5 3 8 6 1 5 5 | 1/31/1995 | Steele et al. | 326 | 37 | | | | | | |
| MN | 5 4 2 6 7 4 4 | 6/20/1995 | Sawase et al. | 395 | 375 | | | | | | |
| MN | 5 5 1 1 2 1 1 | 4/23/1996 | Akao et al. | 395 | 800 | | | | | | |
| FOREIGN PATENT DOCUMENTS | | | | | | | | | | | |
| | Document No. | Date | Country | Class | Sub- Class | Transl. Yes No | | | | | |
| MN | 4 2 0 3 8 8 A 2 | 03.04.91 | EPO | G01R 31/318 | | | | | | | |
| MN | 5 1 0 8 1 5 A 2 | 28.10.92 | EPO | H03K 19/177 | | | | | | | |
| MN | 4 5 5 4 1 4 A 2 | 06.11.91 | EPO | H01L 23/525 | | | | | | | |
| OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.) | | | | | | | | | | | |
| MN | Microcontroller Acceleration, By Jesse Jenkins, 1993 IEEE, pp. 416-424. | | | | | | | | | | |
| | A Family of User-Programmable Peripherals with a Functional Unit Architecture, By A.S. Shubat et al., 1992 IEEE, pp. 515-529. | | | | | | | | | | |
| MN | A User-Programmable Peripheral With Functional Unit Architecture, By A. Shubat et al., pp. 23-24. | | | | | | | | | | |
| MN | A 10ns, 4000 Gate, 160 Pin CMOS EPLD Developed on a 0.8um Process, By R. Patel et al., 1993 IEEE, pp. 7.6.1-7.6.5. | | | | | | | | | | |
| MN | Obtaining 70MHz Performance in the MAX Architecture, By S. Kopec et al., May 1991, pp. 69-74. | | | | | | | | | | |
| Examiner <i>Mike Nguyen</i> | | | Date Considered <i>11/14/02</i> | | | | | | | | |
| Examiner: Initial if references considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. | | | | | | | | | | | |

| | | |
|---|--------------------------------|--------------------------|
| Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | ATTY DOCKET NO. 0325.00372 | SERIAL NO. 09/605,325 |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | APPLICANT: Michael T. Moore | GROUP 2787 |
| | FILING DATE June 28, 2000 | |



RECEIVED
SEP 27 2000
TC 2700 MAIL ROOM

U.S. PATENT DOCUMENTS

| Examiner Initial | Document No. | Date | Name | Class | Sub-Class | Filing Date |
|------------------|---------------|-----------|-------------------|-------|-----------|-------------|
| MN | 5 5 4 8 2 2 8 | 8/20/1996 | Madurawe | 326 | 41 | |
| MN | 5 5 4 8 5 5 2 | 8/20/1996 | Madurawe | 365 | 185.33 | |
| MN | 5 5 5 0 8 4 2 | 8/27/1996 | Tran | 371 | 21.4 | |
| MN | 5 5 5 7 2 1 7 | 9/17/1996 | Pedersen | 326 | 39 | |
| MN | 5 5 7 2 1 4 8 | 11/5/1996 | Lytle et al. | 326 | 41 | |
| MN | 5 5 9 4 3 6 7 | 1/14/1997 | Trimberger et al. | 326 | 41 | |
| MN | 5 5 9 8 1 0 8 | 1/28/1997 | Pedersen et al. | 326 | 41 | |
| MN | 5 6 0 8 3 3 7 | 3/4/1997 | Hendricks et al. | 324 | 765 | |
| MN | 5 7 5 2 0 6 3 | 5/12/1998 | DeRoo et al. | 395 | 800 | |
| MN | 5 7 5 7 2 0 7 | 5/26/1998 | Lytle et al. | 326 | 39 | |
| MN | 5 7 6 0 6 0 7 | 6/2/1998 | Leeds et al. | 326 | 38 | |

FOREIGN PATENT DOCUMENTS


| | Document No. | Date | Country | Class | Sub-Class | Transl. | |
|--|--------------|------|---------|-------|-----------|---------|----|
| | | | | | | Yes | No |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)

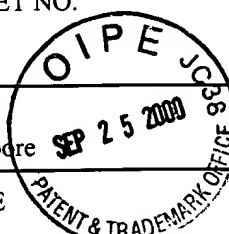
| | |
|----|---|
| MN | SIPPOS (Single Poly Pure CMOS) EEPROM Embedded FPGA by News Ring Interconnection and Highway Path, By K. Ohsaki et al., 1994 IEEE, pp. 9.4.1-9.4.4. |
| MN | Intel's FLEXlogic FPGA Architecture, By D.E. Smith, 1993 IEEE, pp. 378-384. |
| MN | Dual and Fail-Safe Redundancy for Static Mask-ROMs and PLAs, By N. Tsuda, 1993 IEEE, pp. 57-66. |
| MN | A 0.5um Technology for Advanced Microcontroller Applications, By U. Shama et al., 1994 IEEE, pp. 67-68. |
| MN | A Large Scale FPGA with 10K Core Cells with CMOS 08.um 3-Layered Metal Process, By H. Muroga et al., 1991 IEEE, pp. 6.4.1-6.4.4 |

| | |
|----------------------------------|---------------------------------|
| Examiner <i>Michael V. Guyer</i> | Date Considered <i>11/14/02</i> |
|----------------------------------|---------------------------------|

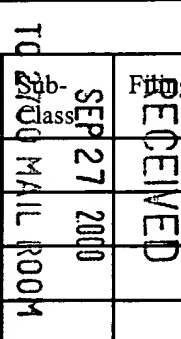
Examiner: Initial if references considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

| Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | ATTY DOCKET NO. 0325.00372 | | SERIAL NO. 10-7-00 09/605,325 | | |
|---|---|--------------------------------|---------------------------------|--|---------------|-------------------|
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | | APPLICANT: Michael T. Moore | | <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;">  </div> <div style="writing-mode: vertical-rl; transform: rotate(180deg);"> RECEIVED SEP 27 2000 TC 270D MAIL ROOM </div> </div> | | |
| | | FILING DATE June 28, 2000 | | | | GROUP 2787 |
| U.S. PATENT DOCUMENTS | | | | | | |
| Examiner Initial | Document No. | Date | Name | Class | Sub- Class | Filing Date |
| MN | 5 7 9 8 6 5 6 | 8/25/1998 | Kean | 326 | 39 | |
| MN | 5 9 9 0 7 1 7 | 11/23/1999 | Partovi et al. | 327 | 210 | |
| MN | 6 0 0 5 8 0 6 | 12/21/1999 | Madurawe et al. | 365 | 185.23 | |
| MN | 6 0 2 3 5 7 0 | 2/8/2000 | Tang et al. | 395 | 500.18 | |
| MN | 6 0 2 5 7 3 7 | 2/15/2000 | Patel et al. | 326 | 80 | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| FOREIGN PATENT DOCUMENTS | | | | | | |
| | Document No. | Date | Country | Class | Sub- Class | Transl. Yes No |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.) | | | | | | |
| MN | Session 15: High-Speed Digital Circuits, FAM 15.5: A 9ns, Low Standby Power CMOS PLD with a Single-Poly EPROM Cell, By S. Frake et al., 2/17/1989, pp. 344-346. | | | | | |
| MN | A Microcontroller Embedded with 4Kbit Ferroelectric Non-Volatile Memory, By T. Fukushima et al., 1996 IEEE, pp. 46-47. | | | | | |
| MN | Integrated Circuits for Smart Cards, By Julie Krueger, 10/9-12/1995, pp. 1168-1170. | | | | | |
| MN | 1.5V High Speed Read Operation and Low Power Consumption Circuit Technology for EPROM and Flash-EERPOM, By O. Matsumoto et al., 1993 IEEE, pp. 25.4.1-25.4.4. | | | | | |
| MN | Integrated Memory Elements on Microcontroller Devices, By Charles Melear, pp. 507-514. | | | | | |
| Examiner | <i>Mitedygen</i> | | Date Considered <u>11/14/00</u> | | | |
| Examiner: Initial if references considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. | | | | | | |

| | | | | | | | |
|---|--|--|--|--------------------------------|--|--------------------------|--|
| Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | | | | ATTY DOCKET NO. 0325.00372 | | SERIAL NO. 09/605,325 | |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | | | | APPLICANT: Michael T. Moore | | GROUP 2787 | |
| | | | | FILING DATE June 28, 2000 | | | |



| U.S. PATENT DOCUMENTS | | | | | | | |
|-----------------------|--------------|------|------|-------|---------------|-------------|--|
| Examiner Initial | Document No. | Date | Name | Class | Sub- Class | Filing Date | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |



| FOREIGN PATENT DOCUMENTS | | | | | | | |
|--------------------------|--------------|------|---------|-------|---------------|---------|----|
| | Document No. | Date | Country | Class | Sub- Class | Transl. | |
| | | | | | | Yes | No |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

| OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.) | |
|--|---|
| MN | Analog Counterparts of FPGAs Ease System Design, By F. Goodenough, 10/14/1994, pp. 63-72. |
| MN | PSD301 Programmable Peripheral With Memory for Microcontroller and Embedded Microprocessor Applications, By Chris Jay, 1991. |
| MN | Single Chip Microcontroller with Internal EPROMs, By M. Yamamoto et al., National Technical Report, Vol. 36, No. 3, June 1990, pp. 295-302. |
| | |
| | |

| | |
|----------------------------|---------------------------------|
| Examiner <i>Mike Ryuga</i> | Date Considered <i>11/15/02</i> |
|----------------------------|---------------------------------|

Examiner: Initial if references considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.